

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Page 1 of 2	ATTY. DOCKET NO. R0998-200B	SERIAL NO. (Unassigned)	APPLICANT: Salvatore N. Storino, et al.
	FILING DATE: Herewith	GROUP: Unassigned 2823	09/751163 12/29/00

REFERENCE DESIGNATION										U.S. PATENT DOCUMENTS			
EXAMINER INITIALS		DOCUMENT NUMBER							DATE	NAME	CLASS	SUB- CLASS	FILING DATE (IF APPRO.)
K.N.	AA	6	0	9	4	0	7	2	7/25/2000	Davies, et al.	326	98	3/16/1999
K.N.	AB	6	0	3	4	3	9	9	3/07/2000	Brady, et al.	257	355	3/06/1997
K.N.	AC	6	0	3	1	2	6	1	2/29/2000	Kang	257	302	7/29/1998
K.N.	AD	6	0	2	8	3	3	7	2/22/2000	Letavic, et al.	257	347	11/06/1998
K.N.	AE	6	0	2	3	0	8	9	2/08/2000	Kang	257	347	8/14/1998
K.N.	AF	6	0	2	0	2	2	2	2/01/2000	Wollesen	438	149	12/16/1997
K.N.	AG	6	0	0	2	2	7	1	12/14/1999	Chu, et al.	326	98	5/12/1997
K.N.	AH	5	9	9	4	7	3	8	11/30/1999	Wollesen	257	347	12/16/1997
K.N.	AI	5	9	8	5	7	2	8	11/16/1999	Jennings	438	311	9/01/1995
K.N.	AJ	5	9	8	2	0	0	6	11/09/1999	Joyner	257	347	12/09/1997
K.N.	AK	5	9	3	2	9	1	4	8/03/1999	Horiguchi	257	355	7/22/1997

FOREIGN PATENT DOCUMENTS														
		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION	
													YES	NO
K.N.	AL	6	2	0	9	1	0	9	7/26/1994	Japan	H01L29	784	Abstract only	
K.N.	AM	6	2	0	4	4	4	0	7/22/1994	Japan	H01L27	12	Abstract only	
K.N.	AN	6	1	1	2	4	8	3	4/22/1994	Japan	H01L29	784	Abstract only	
	AO													
	AP													

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
K.N.	AR	U.S. Patent Application Serial No. 09/239,289, by Storino et al., "Method and Apparatus for Elimination of Parasitic Bipolar Action in Logic Circuits for History Removal Under Stack Contention Including CMOS SOI Elements", filed 1/29/99
		U.S. Patent App Serial No. 09/240,991, by Tran et al., "Method and Apparatus for Elimination of Parasitic Bipolar Action in Logic Circuits Including Complementary Oxide Semiconductor (CMOS) Silicon on Insulator Elements", filed 1/29/99
K.N.	AS	
K.N.	AT	"Pre-Discharge Technique to Improve Noise Immunity on Silicon-on-Insulator (SOI) Domino Circuits", Research Disclosure No. 408, April 1998, pp. 496-97.

EXAMINER <i>Khemnguyen</i>	DATE CONSIDERED <i>9/5/02</i>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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GROUP: Unassigned

2823

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE (IF APPRO.)
K.N.	BA	5 9 2 3 0 7 1	7/13/1999	Saito	257	458	9/27/1993
K.N.	BB	5 9 1 7 3 5 5	7/29/1999	Klass	327	208	1/16/1997
K.N.	BC	5 8 3 1 4 5 1	11/03/1998	Bosshart	326	93	7/19/1996
K.N.	BD	5 7 9 3 2 2 8	8/11/1998	Evans	326	98	1/31/1997
K.N.	BE	5 7 7 7 4 9 1	7/07/1998	Hwang, et al.	326	113	6/10/1996
K.N.	BF	5 7 7 0 8 8 1	6/23/1998	Pelella, et al.	257	347	9/12/1996
K.N.	BG	5 7 4 8 0 1 6	5/05/1998	Kurosawa	327	108	3/20/1996
K.N.	BH	5 7 4 2 0 7 5	4/21/1998	Burns, et al.	257	59	11/18/1996
K.N.	BI	5 6 2 7 3 9 5	5/06/1997	Witek, et al.	257	350	
K.N.	BJ	4 8 9 3 1 5 8	1/09/1990	Mihara, et al.	357	23.13	
	BK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION	
							YES	NO
	BL							
	BM							
	BN							
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